Application Bulletin AB-14

Details of Output Capacitor Selection for Pentium II Processor Converters using the RC5051

Summary

Selecting the proper set of bulk output capacitors for a Pentium II power supply based on the RC5051 requires detailed understanding of both the specs and the IC. Using the calculations provided in this Application Bulletin enables you to select capacitors that will minimize the total cost, while ensuring that the power still meets the transient requirements under worst case.

The Specifications

The first step towards being able to select output capacitors for a Pentium II power supply is to understand the specifications which that supply must meet. The specifications vary between processor types, and even for a single processor type depending on its operating frequency. To be concrete in this Application Bulletin, we will consider the 2.0V Pentium II processors only; other versions may be dealt with in a similar manner.

The power supply specifications fall into two parts: DC regulation and Transient regulation. DC regulation is how well the DC output voltage of the power supply must match its VID programmed level, over component variation, temperature, static load change, etc. Transient regulation is how much the supply's output voltage is allowed to deviate from its programmed level when a (very fast) load step is applied. Clearly transient limits must be broader than DC regulation limits, but in fact they are much harder to meet, depending as they do on both the converter response and the output capacitors.

The DC regulation limits are ±60mV for most speeds. Transient limits are ±100mV for most speeds (the "–" meaning the undershoot when a load is pulsed on, the "+" meaning the overshoot when a load is pulsed off). This means that if a (hypothetical) supply were providing a voltage that was already 60mV high, it would only be allowed to rise an additional 40mV—the transient limits *include* the DC tolerance.

Contributors to DC Regulation

1. The first thing to realize about the RC5051 is that it is trimmed high, that is, when the VID lines are set for 2.000V, the reference voltage of the RC5051 is actually (nominally) 2.020V. (The trim is 2.825V when the VID lines are set for 2.800V.) This is done intentionally in order to compensate for the trace resistance present in typical designs, which causes the output voltage to be lower at the CPU than at the output capacitors. The tolerance on this setting is ±1% = ±20mV (±28mV at 2.8V). Thus the reference plus tolerance stackup is 2.000V - 2.040V.

2. A second contribution to the DC tolerance is the temperature coefficient of the reference voltage, which is +0.0125%/°C. Since the RC5051 when running self-heats, it is safe to assume that only temperatures above ambient need be considered; the change in voltage when the temperature of the die rises from 25°C to 70°C is +0.56%, which is 11mV at 2.0V (16mV at 2.8V).

Table 1. Regulation Specifications for 2.0V Pentium II Converters

Processor Speed (MHz)	Maximum DC Current (A)	DC Limits	Transient Limits
266	8.5	-60mV +100mV	-110mV +110mV
333	10.6	-60mV +60mV	-110mV +110mV
350	11.1	-60mV +60mV	-100mV +100mV
400	12.6	-60mV +60mV	-100mV +100mV
450	14.2	-60mV +60mV	-100mV +100mV
500	16.0	-60mV +60mV	-100mV +100mV

3. Another contribution to the DC regulation is the load regulation of the RC5051. The RC5051 (intentionally) has limited DC gain in its control loop, so that as the current increases, the output voltage drops; this again helps minimize the number of output capacitors required. The drop due to load regulation is 1%, which is 20mV at 2.0V (28mV at 2.8V).

4. A final (optional) contributor to the DC regulation is the presence of a "droop" resistor. This refers to a resistance between the converter's voltage feedback point and the load (see Figure 1).

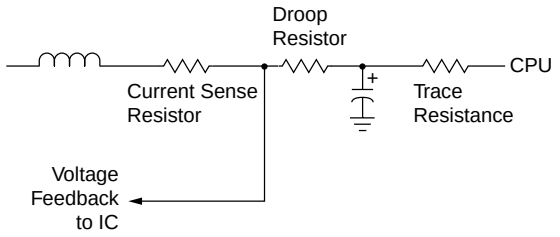

Figure 1. A Droop Resistor is a Resistance Added between the Converter's Regulation Point and the Output Caps to Improve Transient Performance

For small values of this resistance (a few milliohms) the droop resistor can actually improve the converter's transient response: when the load is heavy, the voltage seen by the load is somewhat decreased from what it would otherwise be due to the IR drop of the droop resistor. Thus, for example, when the load suddenly becomes light, there is additional room available for the voltage to surge up.

Note that the droop resistance is the resistance between the current sense resistor and the output caps. This will frequently be present just due to layout constraints on the trace connecting the two. However, it is important that the voltage feedback line to the IC be attached directly at the current sense resistor, *not* on the other side of any droop resistance, as this will affect the current limit.

5. It should also be observed that an effect similar to that of a droop resistor may be induced unintentionally by using too small a trace to conduct the current from the converter's capacitors to the processor. This corresponds in the figure to having a resistor between the output capacitor and the load. Here, however, the droop is bad: when the load transitions from light to heavy, for example, there is an additional drop adding in to the voltage that the CPU sees, potentially taking it outside the regulation range.

We can now sum up all the contributions to DC regulation for a 2.0V Pentium II converter. The highest possible voltage will occur if: 1) The nominal voltage has the tolerance on the trim of +20mV; 2) The temperature of the die is 70°C, which gives 11mV high; 3) The load is at minimum, so that there is no load regulation droop; 4) There is no droop resistance and no trace resistance at all. Summing up all of these terms we get Table 2:

Table 2. Positive DC Regulation Using the RC5051

Effect	2.0V Pentium II
Trim	+20mV
Trim Tolerance	+20mV
Temperature	+11mV
Load Regulation	0
Droop	0
TOTAL	+51mV

These clearly meet the limits of the required DC regulation for all processor speeds.

The lowest possible voltage will occur, conversely, when: 1) The nominal voltage has the tolerance on the trim of -20mV; 2) The temperature of the die is 25°C, which gives no temperature offset; 3) The load is at maximum, so there is a -20mV droop; and 4) Again, with the load at maximum, droop resistance (and unintentional droop due to trace resistance) has an effect of I_{max} x R_{droop}. Summing up all of these terms we get Table 3:

Table 3. Negative DC Regulation Using the RC5051

Effect	2.0V Pentium II
Trim	+20mV
Trim Tolerance	-20mV
Temperature	0
Load Regulation	-20mV
Droop	$-I_{max}$ x R
TOTAL	-20mV - (I_{max} x R)

The spec will be met if

$$-20\text{mV} - (I_{max} \times R) \geq -60\text{mV}$$

which gives the maximum R as detailed in Table 4:

Table 4. Maximum Allowable Droop Plus Trace Resistance for 2.0V Pentium II Converters Using the RC5051

Processor Speed (MHz)	DC Current (A)	Maximum R (mΩ)
266	8.5	4.7
333	10.6	3.8
350	11.1	3.6
400	12.6	3.2
450	14.2	2.8
500	16.0	2.5

Notice that this limit also includes the effect of trace resistance: If the trace from the output of the converter to the processor has more resistance than this, the load regulation requirements CANNOT be met!

Contributors to Transient Regulation

Transient regulation depends on all of the factors that determined DC regulation, and in addition on the ESR of the output capacitors. When the load goes from minimum to maximum, the current cannot come instantaneously from the converter's inductor, and so it comes from the output capacitors; since these capacitors have ESR, the output voltage drops by the factor (change in current x ESR). Similarly, when the load goes from maximum to minimum, the current in the inductor does not instantaneously drop, and so the current goes into the output capacitors, raising the output voltage by (change in current x ESR). Only the ESR is considered here, because in general the capacitance value used is very large, and so the capacitors don't actually charge up any.

Considering first the transition from minimum to maximum output current, the output voltage will dip lowest if: 1) The nominal voltage has the tolerance on the trim of -20mV; 2) The temperature of the die is 25°C, so that there is no rise in output voltage due to heating. Additionally, since we are stepping up to maximum load, 3) Any trace resistance will have an effect of I_{max} x R_{trace}. However, droop resistance will NOT affect the output, because initially (before the transient, while output current is low) the capacitor voltage is equal to the feedback voltage. Note that load regulation droop has no effect here because the converter doesn't respond to the transient in the time frame being discussed here. Finally, 3) The load step will cause a drop due to the ESR of the capacitors of I_{max} x ESR. Summing up all of these terms we get Table 5:

Table 5. Negative Transient Regulation Using the RC5051

Effect	2.0V Pentium II
Trim	+20mV
Trim Tolerance	-20mV
Temperature	0
Load Regulation	0
Trace Droop	$-I_{max} \times R_{Trace}$
ESR	$-I_{max}$ x ESR
TOTAL	$-[I_{max} * (R_{Trace} + ESR)]$

Considering next the transition from maximum to minimum output current, the output voltage will rise highest if: 1) The nominal voltage has the tolerance on the trim of +20mV; 2) The temperature of the die is 70°C, which gives 11mV high. Additionally, since we are stepping down to minimum load, 3) There will be a load regulation droop because initially the converter sees a high current, and 4) Any trace resistance will have no effect immediately after the transition. However, the droop resistor IS effective, because there will be a drop initially from the feedback point to the output caps. Finally, 5) The load step will cause a rise due to the ESR of the capacitors of I_{max} x ESR. Summing up all of these terms we get Table 6:

Table 6. Positive Transient Regulation Using the RC5051

Effect	2.0V Pentium II
Trim	+20mV
Trim Tolerance	+20mV
Temperature	+11mV
Load Regulation	-20mV
Droop	$-I_{max} \times R_{Droop}$
ESR	$+I_{max}$ x ESR
TOTAL	$31mV + [I_{max} \times (ESR - R_{Droop})]$

To satisfy the transient limits we must simultaneously satisfy:

$$-I_{max}(R_{Trace} + ESR) \geq -\text{Transient Limit}$$

and

$$31mV + [I_{max} \times (ESR - R_{Droop})] \leq +\text{Transient Limit}$$

These equations make it clear that a good design should 1) *minimize* the trace resistance between the output capacitors and the CPU, that is *place the output caps as close as possible to the CPU*; and 2) use a droop resistance, which may be just the trace resistance from the current sense resistor to the output caps.

Saving capacitors will mandate using the largest possible ESR. Allowing for no trace resistance and 800μΩ of droop resistance, the latter caused by PCB layout constraints, and as is commonly seen in designs, it turns out that the second equation limits the ESR more than the first for this class of processors; we get limits on the ESR as shown in Table 7:

Table 7. Maximum Allowable ESR for Typical 2.0V Pentium II Converters Using the RC5051 (R_{trace} = 0, R_{droop} = 800μΩ)

Processor Speed (MHz)	ESR_{max} (mΩ)
266	10.1
333	8.3
350	7.0
400	6.3
450	5.7
500	5.1

It is clear from these equations that 1) Trace resistance between the output capacitors and the processor may necessitate using more output caps; and 2) Droop resistance (even unintentional) can decrease the number of capacitors required on the output.

Capacitor Selection

Table 8 presents a partial selection of some commonly used capacitors, showing their ESR and the number of capacitors required to meet the ESR limits for the 2.0V Pentium II, assuming again R_{trace} = 0 and R_{droop} = 800mΩ.

Cautions

Although Table 8 shows the absolute minimum number of capacitors required to meet 2.0V Pentium II specifications using an RC5051 based converter, there are additional considerations that may make adding additional capacitance highly desirable.

1. Any significant trace resistance between the capacitors and the load will degrade the transient response, pushing it out of spec if the absolute minimum number of capacitors is used. Similarly, if the droop resistance turns out to be less than assumed here, the spec will also be violated. For that matter, there is trace resistance connecting the capacitors together, and this also acts as ESR. Even the *solder joints* for through-hole components typically run 0.2mΩ, and so add to the ESR.

2. The effect of capacitor ESL has been ignored here. This inductance causes a large swing in output voltage for a short time. Although Intel specs allow for a 2μsec deviation outside of spec range to cover this problem, additional capacitance might be good to mitigate it.

3. The effect of charge drain on the output capacitors has been assumed negligible in this computation. Especially when extremely low ESR capacitors (such as the Sanyo 820μF Oscon capacitors in Table 8) are used, there may be so little capacitance that the voltage dips down further due to discharge.

For these reasons, it is better to leave a little margin in the number of capacitors used; as a rule of thumb, Fairchild Applications suggests adding one additional capacitor on the output beyond those specified in Table 8.

Table 8. Minimum Number of Some Common Capacitors Required to Meet Pentium II Transient Regulation with an RC5051 Converter

Manufacturer	Part Number	ESR(mΩ)	Number Required for 2.0V Pentium II					
			266MHz	333MHz	350MHz	400MHz	450MHz	500MHz
Sanyo	6MV1500GX	44	5	6	7	7	8	9
Sanyo	4SP820M	12	2	2	2	2	3	3
Panasonic	EEUFA06152	52	6	7	8	9	10	11

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